REMARKS

Claims 1 to 32 stand variously rejected in the outstanding official action. Claim 32 has been cancelled without prejudice and claims 21 and 31 amended. Therefore claims 1-31 are the only claims remaining in this application.

The Examiner's acknowledgement of applicant's claim for priority and receipt of the certified copies of the priority document is very much appreciated. Additionally, the Examiner's indication of the acceptance of the formal drawings is as previously submitted is appreciated. It is noted that applicant discovered a minor error in figure 8E in that R2 should actually be R1. Applicant submits herewith a proposed substitute sheet of drawings implementing this correction.

The Examiner suggests in section 1 of the official action that the title of the invention is not descriptive. The applicant has proposed a substitute title which is believed to be more descriptive of the claimed invention. However, if the examiner is of the opinion that a different title would be more descriptive, he is respectfully requested to provide applicant with such suggestion and it will be considered.

Claims 21-32 stand rejected under 35 U.S.C. § 101 as allegedly being directed to non-statutory subject matter. The Examiner has proposed minor amendments to claims 21 and 31 and those minor amendments have been implemented above. The Examiner proposed cancellation of claim 32 and that suggestion has been implemented above. Accordingly, any further objection or rejection of claims 21-32 under 35 U.S.C. § 101 is respectfully traversed.

Claims 1-9, 11-19 and 21-29 stand rejected under 35 U.S.C. § 102 as being anticipated by Hitt (U.S. Patent 3,654,448). The Hitt reference is concerned with a similar problem as is the present invention, i.e., the operation of transfer instructions for example, load instructions used to

load data values from memory into registers into a register file or store instructions used to store data values from registers of the register file to addresses in the memory. Applicant's specification between pages 2 and 4 discusses a number of techniques which are known which enable a single instruction to specify a multiple loads or stores (multiple transfers between registers and memories). However as specifically discussed in applicant's specification on page 4, line 29 to page 5, line 10 the known techniques making use of a single instruction place significant constraints on the registers that can be identified and used in each transfer. In all such systems, the choice of the register for the first transfer limits the choices available for any subsequent transfer.

The Hitt patent is no exception to the above rule with respect to known prior art systems. While Hitt is generally concerned with providing techniques for improved error recovery by efficient and selective skipping of arithmatic and logic functions in the reexecution of particular instructions (see column 2, lines 9-11), it does contain a reference to load multiple and store multiple instructions (column 4, lines 32-33).

The Examiner suggests that claim 1 is not novel over Hitt, and in arguing this point references the ten lines in column 4, between lines 60 and 70. As specifically described in Hitt at column 4, lines 60-66 described load multiple (LM) and store multiple (STM) instructions transfer signals between a series of general purpose system registers and corresponding locations in system memory. As discussed, the first register in the series is denoted by the R1 quantity and the last register in the series is denoted by the R3 quantity. As stated explicitly in column 4, line 70-column 5, line 3, for either the LM or STM instructions, the series of registers are identified by implementing R1 for each transfer until the number in R1 equals the number in R3. In other words, if R1 actually identifies register 1 and R3 actually identifies register 3 then the LM or

STM instructions involves three transfers; i.e., first transfer being to or from register 1, a second transfer being to or from register 2, and a third transfer being to or from register 3. For each transfer, the address is incremented as shown in blocks 22a or 22b of Figure 3 and discussed in Hitt in column 5, lines 4-13.

Accordingly, just like the prior art LDRD and STRD instructions discussed on page 4 of the present application, the Hitt LM and STM instructions suffer from the limitation that each transfer in the sequence has to take place with respect to adjacent registers. For example, if the first transfer is with respect to register 2 the next transfer has to be with respect to register 3 and the one after that has to be with respect to register 4. This is the the constraint noted in applicant's specification which makes it difficult for software to be written so that it can always take advantage of such instructions (see the disadvantages of the prior art discussed on page 4, lines 22-25 of the present application).

In accordance with applicant's claimed invention, a single transfer and instruction is specified to cause the data processing unit to perform multiple data value transfers between multiple registers and data value addresses in the memory. In accordance with the present invention, the single transfer instruction provides, for each of the data value registers, a register identifier identifying the register which is the subject of that data value transfer. This is specifically enumerated in applicant's independent claim 1 in the last two lines which state "said register identifier for each of said data value transfers being specifiable independently of the register identifiers specified for the other of said data value transfers.

As discussed in applicant's specification page 6, lines 7-10, the claimed arrangement provides a great deal of flexibility in use of the single transfer instruction and allows

significantly more occurrences of multiple separate instructions, each used to transfer one data value to be replaced by this new single transferred instruction.

The invention's flexibility is illustrated in the discussion on page 6, lines 11-18 when comparing the claimed invention with the known prior art. In particular, shown are examples of two standard load instructions and an indication as to whether those load instructions can be replaced by a single load instruction (in an embodiment of the present invention) and whether they can be replaced by a known prior art single load instruction (they cannot).

There is no indication in the Hitt reference that the register identifiers are specified independently of register identifiers for the other of the data value transfers. Using the analogy in the Hitt reference, if the claim 1 first data transfer is in respect to register 2, there is no requirement that the next data transfer be in respect of register 3. Thus, when compared with prior art techniques, the single transfer instruction used in accordance with the present invention provides significantly more scope for replacing a series of instructions.

Claim 1 which positively recites this clear distinction, over the prior art Hitt reference, is clearly patentable over Hitt. Similarly, independent claims 11 and 21 contain the same statement and are therefore similarly patentable over the Hitt reference. As a result, claims 1, 11 and 21 are clearly patentable in view of the Hitt reference, as a consequence the rejection of claims 1-9, 11-19 and 21-29 under U.S.C. § 102 is respectfully traversed.

Claims 6, 10, 16, 20, 26 and 30-32 stand rejected under U.S.C. § 103 as unpatentable over Hitt. In view of the fact that each of these dependent claims depends from one of claims 1, 11 and 21, these are believed patentable for the same reasons noted above in conjunction with the discussion of the anticipation rejection over Hitt, said discussion incorporated by reference.

While claim 32 has been cancelled without prejudice, for the above reasons claims 6, 10, 16, 20, 26, 30 and 31 are not anticipated, are not obvious in view of the Hitt reference.

Moreover, as noted above, the Hitt reference actually teaches away from applicant's invention, i.e., Hitt specifically requires that instructions be incremented or decremented consecutively and this would lead one of ordinary skill in the art away from applicant's register identifiers which are independent of any other register identifier. Accordingly, because Hitt teaches away from applicant's invention, it cannot possibly render obvious applicant's claimed invention.

Having responded to all objections and rejections set forth in the outstanding official action, it is submitted that remaining claims 1-31 are in condition for allowance and notice to that effect is respectfully solicited. In the event the Examiner is of the opinion that a brief telephone or personal interview will facilitate allowance of one or more of the above claims, he is respectfully requested to contact the applicant's undersigned representative.

Respectfully submitted,

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AMENDMENTS TO THE DRAWINGS

The attached sheet (6/6) of drawings includes changes to Fig. 8D. This sheet, which includes Fig. 8D, replaces the original sheet (6/6) including Fig. 8D. In Figure 8D, the previous element LDR R2 has been changed to LDR R1.

Attachment: Replacement Sheet
Annotated Sheet Showing Changes

```
LDR  R0, [R4, #0]   { LDMIA      R4, {R0, R1}
LDR  R1, [R4, #4]   { LDRD       R0, [R4, #0]
                    { LDRD_NEW   R0, R1, [R4, #0]
```

FIG. 8A

```
LDR  R0, [R4, #8]   { X    LDMIA
LDR  R1, [R4, #12]  { LDRD       R0, [R4, #8]
                    { LDRD_NEW   R0, R1, [R4, #8]
```

FIG. 8B

```
LDR  R0, [R4, #0]   { LDMIA      R4, {R0, R2}
LDR  R2, [R4, #4]   { X    LDRD
                    { LDRD_NEW   R0, R2, [R4, #0]
```

FIG. 8C

```
LDR  R2, [R4, #4]   { X    LDMIA
LDR  R0, [R4, #8]   { X    LDRD
                    { LDRD_NEW   R2, R0, [R4, #4]
```

FIG. 8D

```
LDR  R0, [R4, #12]  { X    LDMIA
LDR  ~~R2~~ R1, [R4, #16]  { X    LDRD
                    { LDRD_NEW   R0, R1, [R4, #12]
```

FIG. 8E

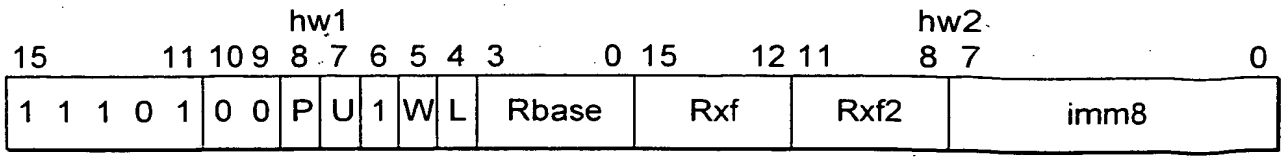

FIG. 9